REMARKS/ARGUMENTS

Claims 1-24 are pending. Claims 1, 5, 10 and 16 have been amended, and claims 2-3, 6-7, and 12-13 have been canceled.

Claims 1-19 stand rejected under 35 U.S.C. §102 (b) as being anticipated by U.S. Patent No. 5,616,510 to *Wong*. Applicants submit that amended claims 1, 5, 10, and 16 are now in condition for allowance and reconsideration to that end is respectfully requested. Specifically, Applicants traverse Examiner's previous rejections, noting that none of the Examiner's references discloses every element of the amended claims. For example, none of the references discloses a tunnel oxide material between the tip of a floating gate and a control gate to permit Fowler-Nordheim tunneling of charges from the floating gate to the control gate, a contact in a first region of a first section in a trench electrically connected to the first region of a second section in the trench, or a first cell in a first row of an array including a first contact in a trench electrically connected to a first region of the cell and electrically connected to the first region of a second cell in a second row of the array.

Wong discloses methods of making vertical stacked gate memory cells according to several embodiments. One embodiment of *Wong* discloses a vertical stacked gate memory cell having a separate tunnel oxide layer between a floating gate and drain of the cell, wherein the memory cell is erased by tunneling charges through the tunnel oxide layer from the floating gate to the drain. (*Wong*, col. 7, lines 10-25; Fig. 6). Other embodiments of *Wong* disclose vertical stacked gate memory cells having a drain (Figs. 5), an extended drain region (Figs. 7), a separate erase/program gate (Figs. 8), or a series select transistor (Figs. 9). In all embodiments, *Wong* discloses tunneling from a floating gate to one of these regions – i.e., to a drain (Figs. 5, col. 7, line 5-7; Figs. 6, col. 7, lines 13-15), to an extended drain (Figs. 7, col. 7, lines 53-55), to an erase/program gate (Figs. 8-9, col. 7, lines 58-61) – to effect erasure of the memory cell. In other words, *Wong* only discloses a tunnel oxide between a floating gate and a drain, or tunneling from a floating gate to one of the abovementioned regions.

The Examiner asserts that *Wong* discloses a tunnel material between the tip of a floating gate and a control gate, wherein the tunnel material is a tunnel oxide configured to permit Fowler-Nordheim tunneling of charges from the floating gate to the control gate. (Office Action of 09/07/2005, pg. 4-5). However, the section cited by the Examiner only discloses an oxide material between the floating gate and control gate, trench, source, drain, and erase/program gate, and not a tunnel material. (Figs. 23, 2310 and 2308; col. 20, lines 23-61). Furthermore, Applicants draw Examiner's attention to the fact that *Wong* uses an erase/program gate, extended drain, or tunnel oxide between drain and floating gate to thicken the oxide material and improve yield and reliability during erasure. (i.e., col. 7, lines 20-25, 50-53). In other words, *Wong* prevents tunneling between the floating gate and other elements of the cell (such as the control gate) by thickening the oxide material around the floating gate. Thus, *Wong* does not disclose a tunnel oxide between the floating gate and control gate, or tunneling of charges from the floating gate to the control gate, as recited in the claims.

In contrast, independent claims 1, 5, 10, and 16 all recite the limitation of a tunnel material between the tip of a floating gate and a control gate, wherein the tunnel material is a tunnel oxide and configured to permit Fowler-Nordheim tunneling of charges from the floating gate to the control gate. As discussed above, *Wong* does not disclose this limitation, and thus does not disclose every element of the claims. Accordingly, claims 1, 5, 10, and 16 are patentable over *Wong* for at least these reasons.

Claim 5 additionally recites the limitation of a first contact in a first trench electrically connected to the first region of a first section and electrically connected to the first region of a second section in the first trench. Similarly, claim 10 recites the limitation of a first cell in a first row including a first contact in the trench electrically connected to the first region of the cell, and electrically connected to the first region of a second cell in a second row separated from the first

row by at least one isolation row. *Wong* fails to disclose any such contact. Accordingly, claims 5 and 10 are patentable over *Wong* for at least these additional reasons.

Therefore, claims 1, 5, 10, and 15 are patentable over *Wong* for at least the aforementioned reasons. Similarly, claim 4 depending from claim 1, claims 8-9 depending from claim 5, claims 11, 14-15 depending from claim 10, and claims 17-19 depending from claim 16, are also patentable over *Wong* for at least these reasons.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

The Examiner is invited to call Applicants' attorney at the telephone number listed below in order to expedite prosecution of this application.

The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to **Deposit Account No. 07-1896** and reference **Attorney Docket No. 351913-992740**.

Respectfully submitted,

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Dated: November 23, 2005

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